

# HA12133MP

## PRE, REC, Equalizer IC for R-DAT

### Description

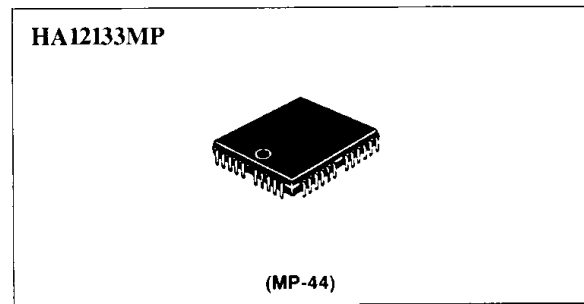
The HA12133MP is a bipolar IC developed for R-DAT (rotary head digital audio tape recorder). It incorporates a playback amplifier, equalizer amplifier, and recording amplifier on one chip.

### Functions

- Playback amplifier
- Equalizer amplifier
- Recording amplifier
- Interface logic

### Features

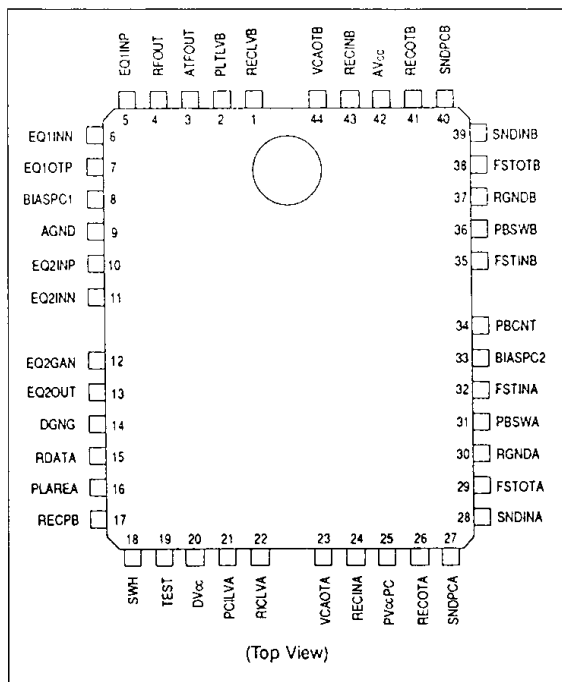
- Incorporates a switching circuit for ATF PILOT area recording level.
- Makes possible direct interface connection to CMOS LSI.
- Allows two kinds of waveform equalizing circuits to be constructed.
- Operates on 5 V single power supply voltage.
- Allows board miniaturization through small surface mount package.



### Ordering Information

Type No.	Package
HA12133MP	MP-44

### Pin Arrangement



# HA12133MP

**Table 1 Absolute Maximum Ratings (Ta = 25 °C)**

Item	Symbol	Rating	Unit
Supply voltage	Vcc	6.0	V
Allowable dissipation	Pd	600	mW
Operation temperature	Topr	-20 to +75	°C
Storage temperature	Tstg	-55 to +125	°C

The absolute maximum ratings are limiting values, to be applied individually, beyond which the device may be permanently damaged. Functional operation under any of these conditions is not guaranteed. Exposing a circuit to its absolute maximum rating for extended periods of time may affect the device's reliability.

**Table 2 Electrical Characteristics (Ta = 25 °C, Vcc = 5.0 V)**

Item	Symbol	Min	Typ	Max	Unit	Test conditions
Operating voltage	Vcc	4.5	5.0	5.5	V	
Current dissipation 1	IccPB	—	35	49	mA	No signal during PB
Current dissipation 2	IccREC	—	46	60	mA	No signal during REC
Preamp voltage gain	GvPRE	58.5	63	67.5	dB	f = 1 MHz, external transistor
Preamp Ach/Bch gain difference	ΔGvPRE	-1.5	0	1.5	dB	Ach - Bch
Preamp band width	BWPRE	—	13	—	MHz	
Preamp input conversion noise voltage	Vn	—	0.8	—	nV/√Hz	Input short, f = 5 MHz, external transistor
Preamp maximum output voltage	VoPRE	1.0	—	—	Vp - p	
EQ1 voltage gain	GvEQ1	21.5	25	28.5	dB	
EQ1 band width	BWEQ1	—	1.5	—	MHz	
EQ1 maximum output voltage	VoEQ1	1.0	—	—		
EQ2 voltage gain 1	GvEQ21	21.0	24.5	28.0	dB	f = 1 MHz, R = 8.2 kΩ
EQ2 voltage gain 2	GvEQ22	16.2	19.7	23.2	dB	f = 1 MHz, R = 16 kΩ
EQ2 band width	BWEQ	—	30	—	MHz	
EQ2 maximum output voltage	VoEQ2	1.0	—	—		



**Electrical Characteristics (Ta = 25 °C, Vcc = 5.0 V) (cont)**

Recording amp current gain	GiREC	36.4	39.4	42.4	dB	f = 1 MHz
Recording amp max output voltage	IoREC	20	—	—	mApp	
VCA maximum output voltage	VoVCA	400	740	—	mVpp	R = 0 Ω
Interface input high level	VIH	3.5	—	—	V	
Interface input low level	VIL	—	—	1.0	V	
Interface input high current	IiH	—	—	100	μA	VIH = 5 V
Interface input low current	IiL	-10	—	—	μA	VIL = 0 V

**Table 3 Pin Functions**

No.	Name	I/O	Function	Equivalent circuit	Connected to
1	RECLVB	—	Resistor connecting pin for setting Bch PCM area recording level		
2	PLTLVB	—	Resistor connecting pin for setting Bch ATF PILOT area recording level		

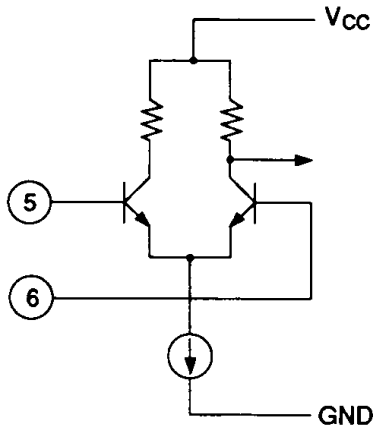
3	ATFOUT	O	Pre-amp output pin for servo LSI		HD49212
4	PFOUT	O	Pre-amp output pin		HA12133MP Equalizer circuit

# HA12133MP

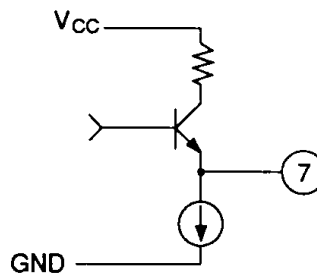
## Pin Functions (cont)

5 EQ1INP I EQ1 normal rotation input pin

6 EQ1INN I EQ1 inversion input pin



7 EQ1OTP O EQ1 output pin



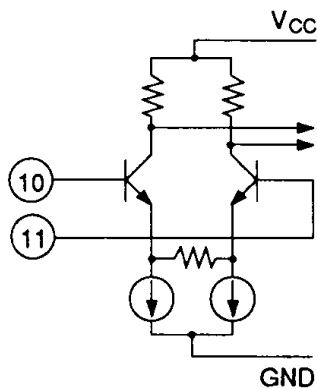
8 BIASPC1 — Bypass condenser connecting pin of bias circuit

9 AGND — Analog GND pin

GND

10 EQ2INP I EQ2 normal rotation input pin

11 EQ2INN I EQ2 inversion input pin

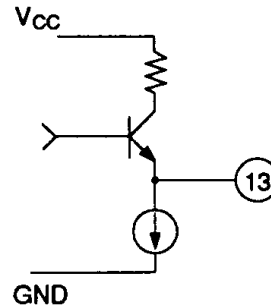


12 EQ2GAN — Resistor connecting pin for setting of EQ2 gain

Pin Functions (cont)

13 EQ2OUT O EQ2 output pin

HA12062AMP



14 DGND — Digital GND pin

GND

15 RDATA I Recording data input pin

HD49211

16 PLAREA I ATF PILOT area recording level switching signal input pin  
"High": PILOT area  
"Low": Other

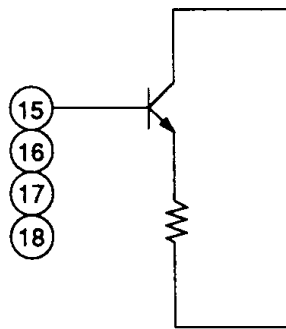
HD49211

17 RECPB I REC/PB switching signal input pin  
"High": Recording  
"Low": Playback

HD49211

18 SWH I Head switching signal input  
"High": Bch  
"Low": Ach

HD49212



19 TEST — Test pin connected to GND

20 DVCC — Digital power supply pin

+5 V

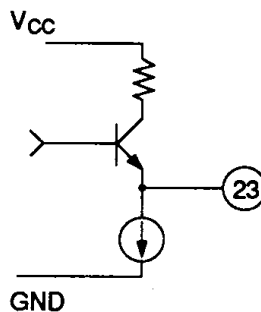
21 PLTLVA — Resistor connecting pin for setting Ach ATF PILOT area recording level

22 RECLVA — Resistor connecting pin for setting Ach PCM area recording level

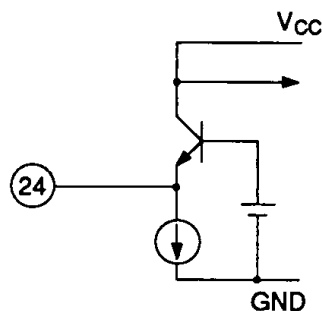
# HA12133MP

## Pin Functions (cont)

23 VCAOTA ○ Ach REC VCA output pin

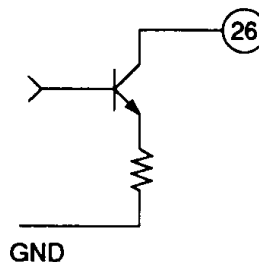


24 RECINA I Ach REC amp input pin



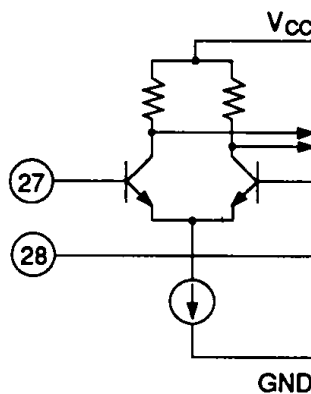
25 PVCCPC ○ Reference output pin

26 RECOTA ○ Ach REC amp output pin



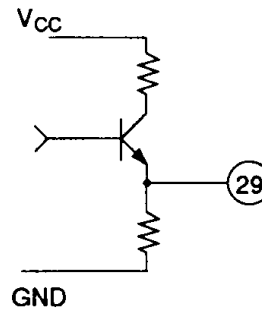
27 SNDPCA — Bypass condenser connecting pin of Ach 2nd amp

28 SNDINA I Ach 2nd amp input pin



**Pin Functions (cont)**

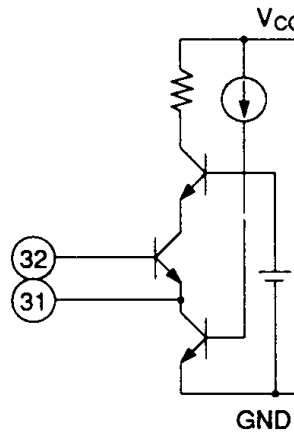
29 FSTOTA ○ Ach 1st amp output pin



30 RGNDA — GND pin GND

31 PBSWA — Ach 1st amp ON/OFF transistor collector pin

32 FSTINA I Ach 1st amp input pin

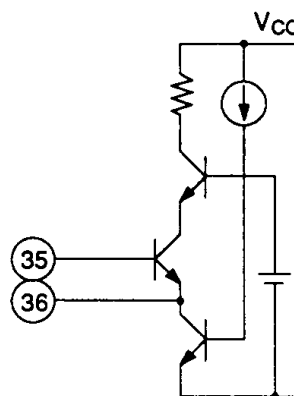


33 BIASPC2 — Bypass condenser connecting pin of bias circuit

34 PBCNT — Base pin of 1st amp ON/OFF transistor

35 FSTINB I Bch 1st amp input pin

36 PBSWB — Collector pin of Bch 1st ON/OFF transistor

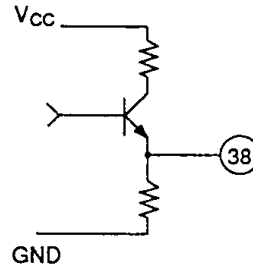


37 RGNDB — GND pin GND

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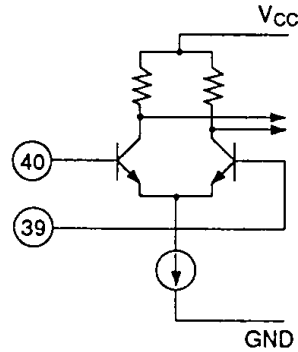
## Pin Functions (cont)

38 FSTOTB ○ Bch 1st amp output pin

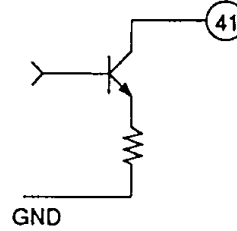


39 SNDINB | Bch 2nd amp input pin

40 SNDPCB — Bypass condenser connecting pin of Bch 2nd amp

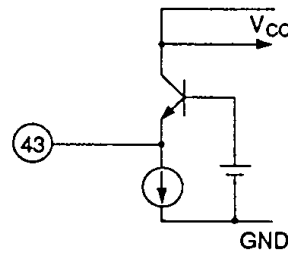


41 RECOTB ○ Bch REC amp output pin

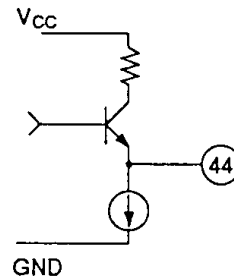


42 AVcc — Analog power supply pin

43 RECINB | Bch REC amp input pin



44 VCAOTB ○ Bch RECVCA output pin







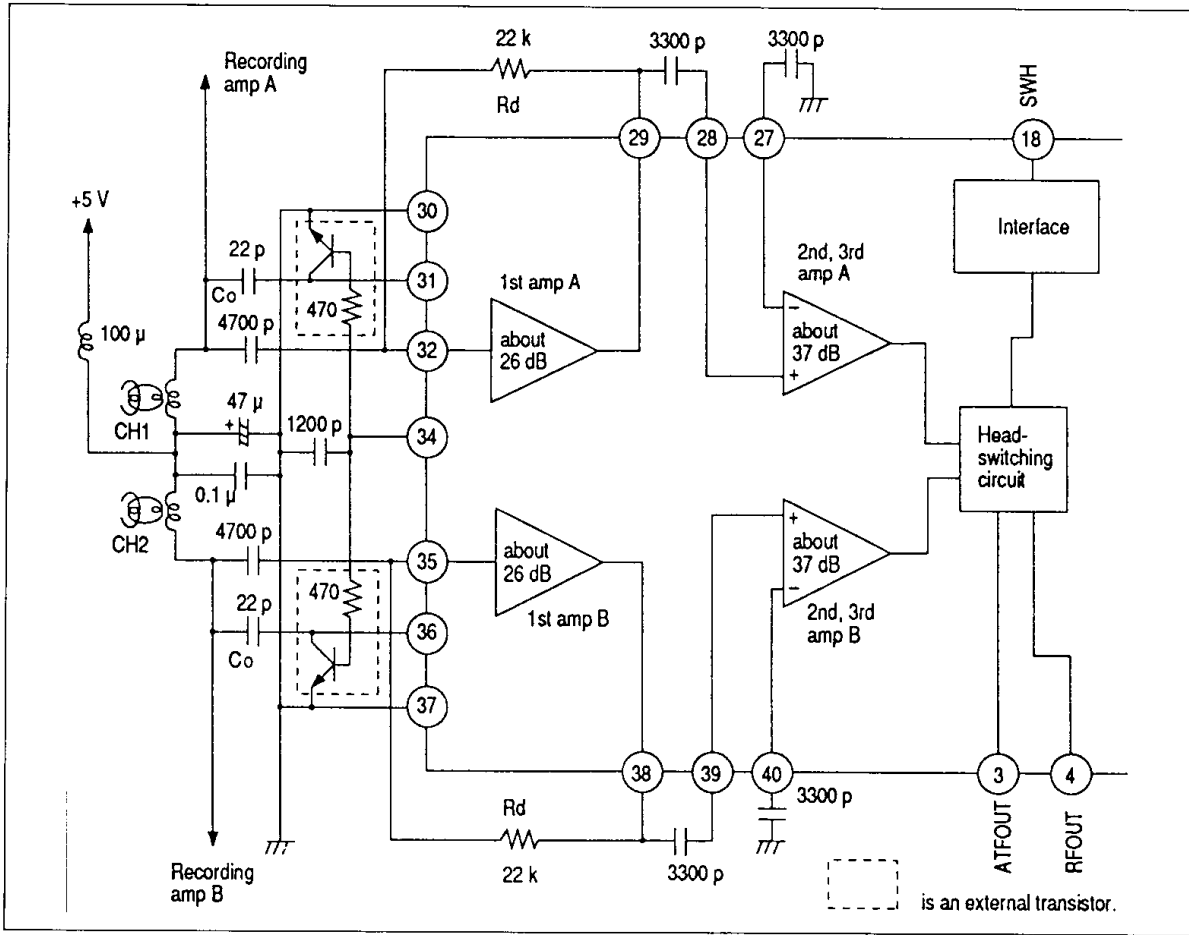


Figure 1 Playback Block

**Equalizer circuit**

The ideal tape to head transmission circuit would exhibit differentiation characteristics. However, actual frequency characteristics exhibit a curve which falls in the high-frequency region, as shown in figure 2.

Intersymbol interference is caused by the high recording density of R-DAT.

The equalizer circuit corrects deteriorated playback signal characteristics and waveform equalizes the entire circuit so that group delay characteristics without intersymbol interference become flat transmission characteristics.

In the HA12133MP, two kinds of equalizer circuits, a CR-type equalizer and a reflector-type transversal equalizer can be constructed for obtaining equalizer characteristics. Therefore, this IC incorporates only two amplifier (EQ1 and EQ2)

which are used in the equalizer circuit. Since the required gain depends on the types of equalizer, EQ2 gain can be freely set to between about 15 dB and 30 dB.

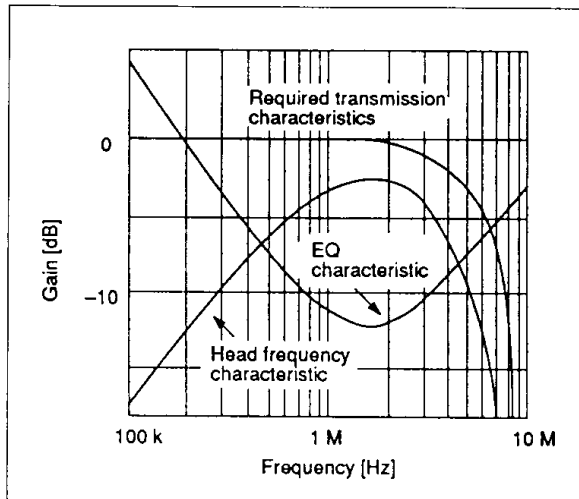
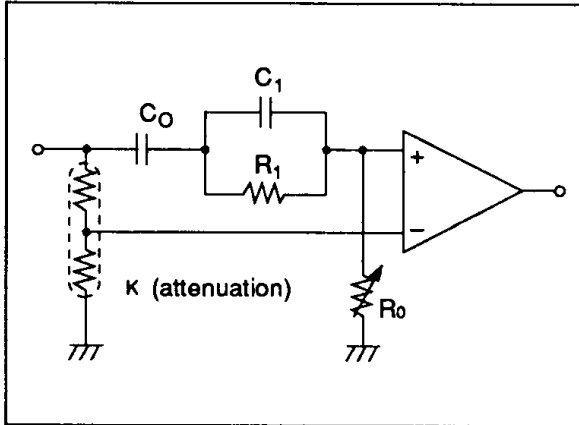
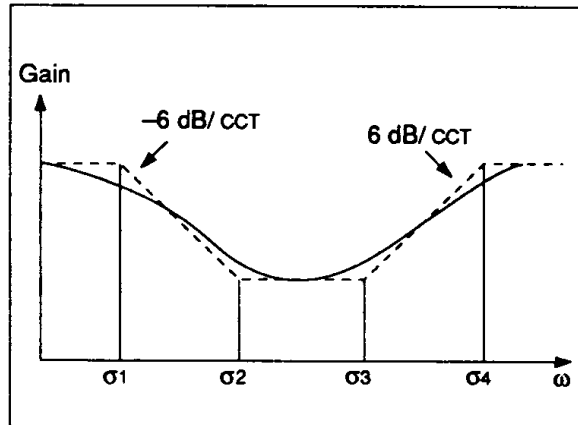


Figure 2 Equalizer Characteristics

**CR-type equalizer:** The CR-type equalizer can obtain equalizer characteristics with only an EQ2 and a few external condensers and registers.



**Figure 3 CR-type Equalizer**



**Figure 4 CR-type Equalizer Amplitude Characteristic**

The CR-type equalizer configuration shown in figure 3 produces the characteristic shown in figure 4. This characteristic is expressed as

$$H(S) = \frac{(S + \sigma_2)(S - \sigma_3)}{(S + \sigma_1)(S + \sigma_4)} \dots\dots\dots (1)$$

By making  $\sigma_2 = \sigma_3$  in formula (1),

$$H(S) = \frac{(S^2 - \sigma_2^2)}{(S + \sigma_1)(S + \sigma_4)} \dots\dots\dots (2)$$

is obtained, and the group delay characteristics around  $\sigma_2 (= \sigma_3)$  become flat.

Each of the external constants of the CR-type equalizer is defined according to the following formula.

$$\sigma_0 = \frac{\sigma_1 \cdot \sigma_4 (\sigma_2 - \sigma_3) + \sigma_2 \cdot \sigma_3 (\sigma_1 + \sigma_4)}{\sigma_1 \cdot \sigma_4 + \sigma_2 \cdot \sigma_3}$$

$$h_0 = \frac{\sigma_1 \cdot \sigma_4}{\sigma_0}$$

$$h_1 = \frac{(\sigma_1 + \sigma_4 - \sigma_0) \sigma_0 - \sigma_1 \cdot \sigma_4}{\sigma_0}$$

$$C_0 = \frac{1}{h_0 \cdot R_0} [F]$$

$$C_1 = \frac{1}{h_1 \cdot R_0} [F]$$

$$R_1 = \frac{h_1}{\sigma_0} \cdot R_0 [\Omega]$$

$$K = \frac{\sigma_2 \cdot \sigma_3}{\sigma_1 \cdot \sigma_4 + \sigma_2 \cdot \sigma_3} \quad R_0: \text{Adjustment}$$

The disadvantage of the CR-type equalizer is that the band extends above the required band width resulting in a poor S/N ratio. Therefore, EQ1 should be used to form a second low-pass filter to reduce noise outside the required band width.

Figure 5 gives an example of a typical CR-type equalizer. The value of each constant is obtained when each corner of the equalizer characteristic is set at  $f_1 = 70 \text{ kHz}$ ,  $f_2 = f_3 = 700 \text{ kHz}$ ,  $f_4 = 7 \text{ MHz}$  and  $R_0 = 1 \text{ k}\Omega$ . The calculated value, therefore, becomes  $C_0 = 1148 \text{ pF}$ ,  $C_1 = 46.9 \text{ pF}$ ,  $R_1 = 960.8 \Omega$ , and  $k = 0.5$ . Cutoff frequency  $f_c$  of the EQ1 low-pass filter is about 6.5 MHz. Rough frequency characteristics are shown in figure 6.



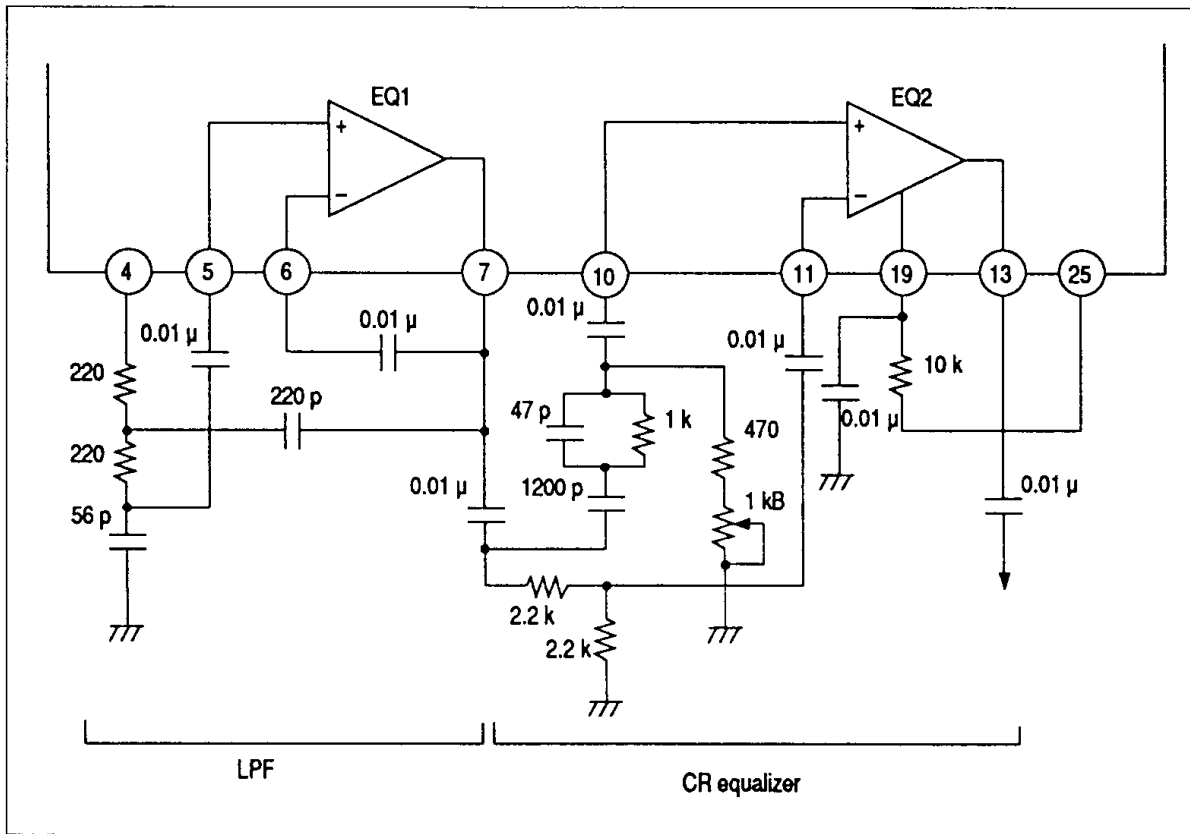


Figure 5 CR-type Equalizer Configuration

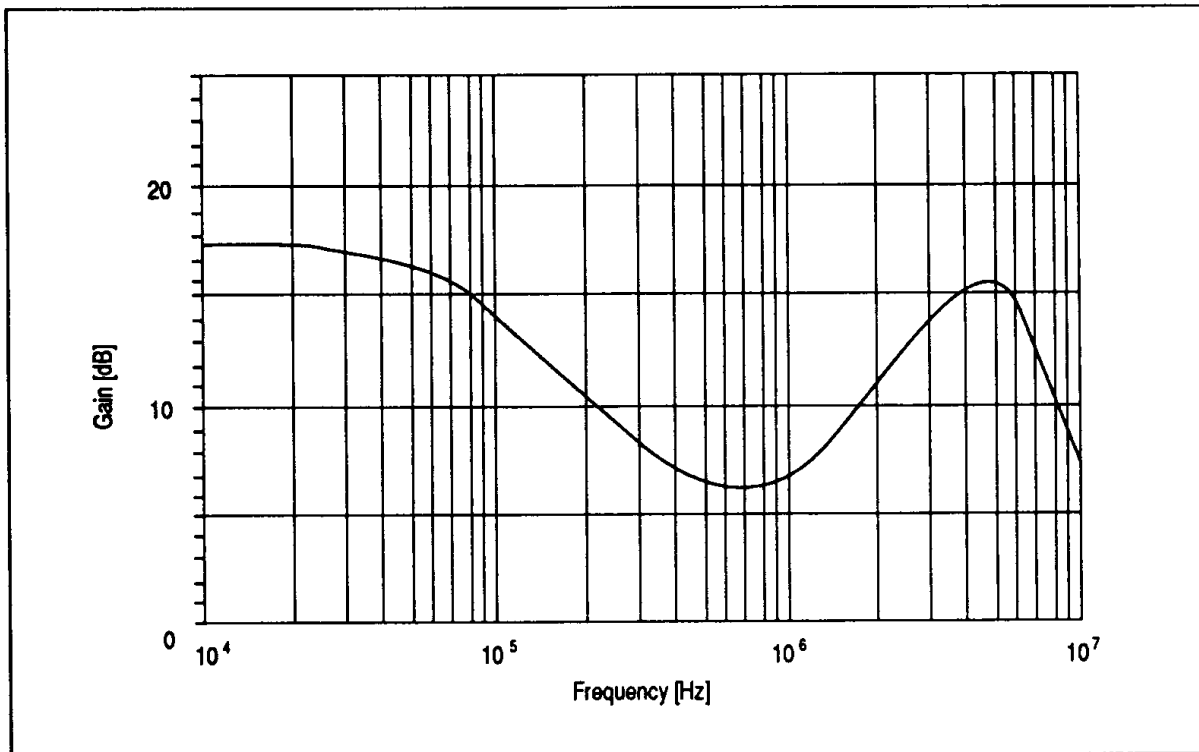


Figure 6 CR-type Equalizer Frequency Characteristics

**Reflector-type transversal equalizer:** The reflector-type transversal equalizer is made up of an integrating circuit which eliminates low-

frequency head differential characteristics and a three-tap transversal filter which corrects high-frequency characteristics.

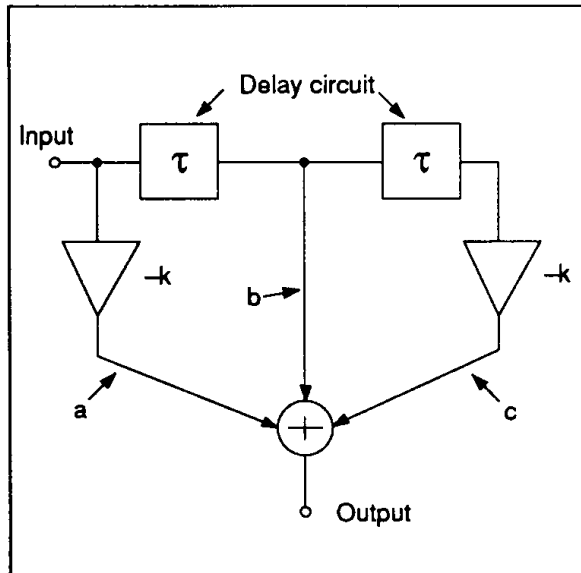


Figure 7 Three-tap Transversal Filter

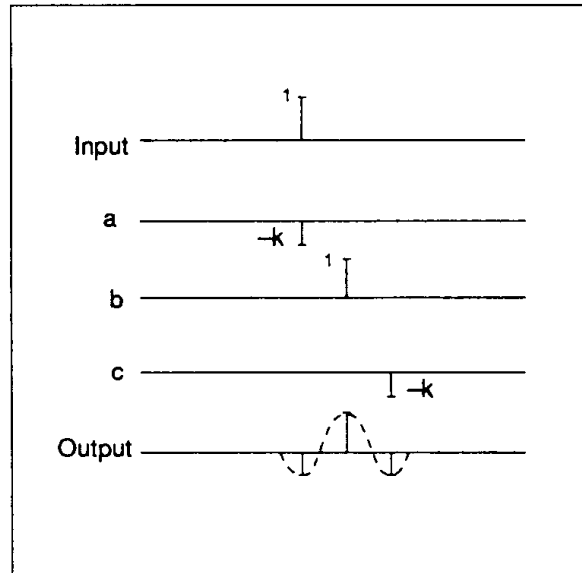


Figure 8 Transversal Filter Operating Principle

The operating principle of the three-tap transversal filter is shown in figure 8. The band-pass filter is formed by multiplying each the advanced response waveforms and the delayed response waveform for period  $\tau$  by  $-\kappa$  and adding them to the original response. By combining this band-pass filter with the integrating circuit, group delay characteristics can be given flat equalizer characteristics.

Figure 10 gives an example of a standard reflector-type transversal equalizer. EQ1 constitutes an integrating circuit and EQ2 constitutes a reflector-type three-tap transversal filter.

HA12133MP reduces the number of external components by using this reflector-type transversal filter, which has only one delay circuit.

The reflector-type three-tap transversal filter can operate as an equalizers although it has only one delay circuit as shown in figure 9. This is because the input impedance of the amplifier is so high that the reflection coefficient is about 1 when the amp is regarded as a transmission line. Therefore, the delay circuit and  $R_k$  are used twice so as to operate as a three-tap transversal filter. And impedance matching should be carried out at point A to prevent unnecessary reflection.

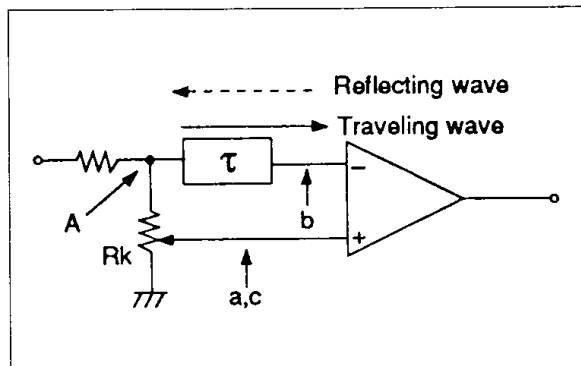


Figure 9 Reflector-type Three-tap Transversal Filter Operation

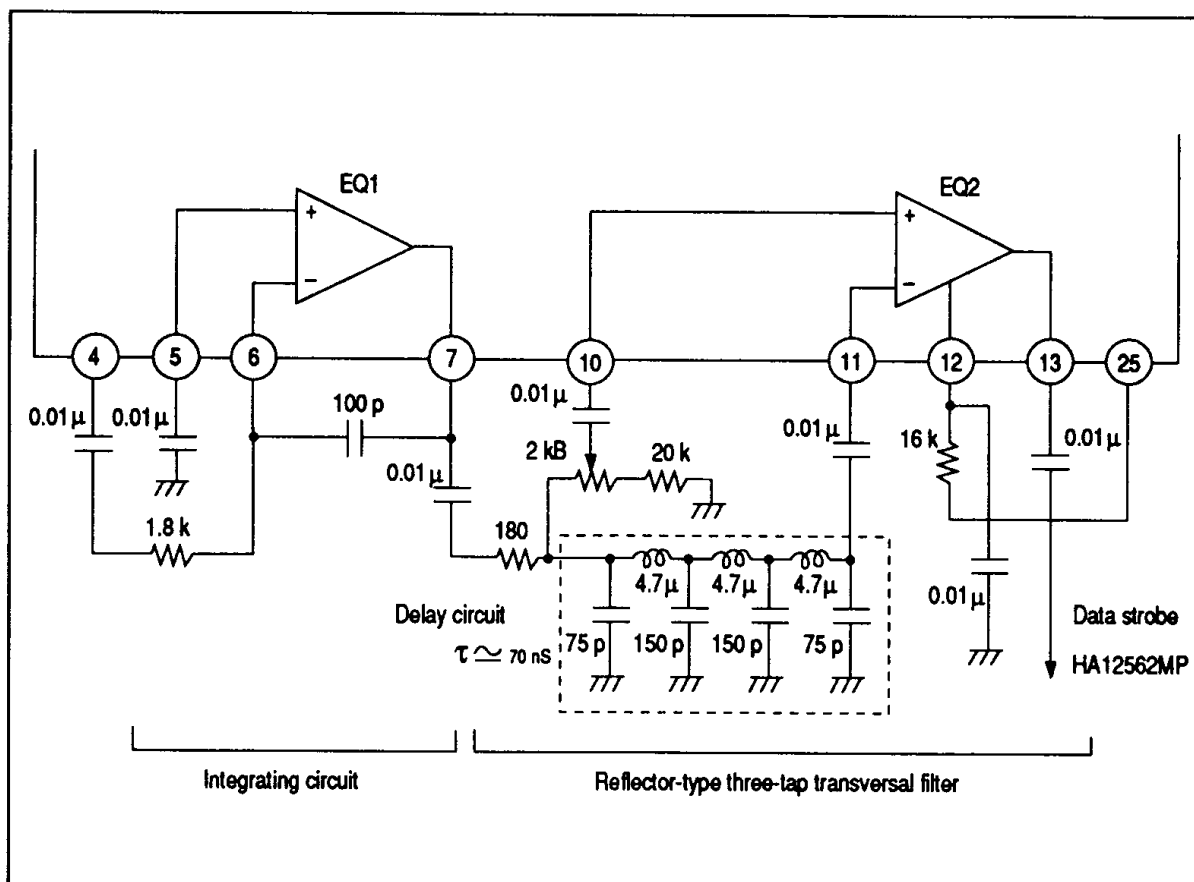


Figure 10 Reflector-type Transversal Equalizer Configuration

**Recording Block**

This circuit block drives the rotary transformer which is connected to the head so that the recording data, modulated 8 to 10 by signal processing LSI HD49211, is recorded on the magnetic tape.

The recording block has an Ach and Bch, each of which are comprised of REC VCA and recording amplifiers.

**REC VCA (Voltage Controlled Amplifier)**

In R-DAT, the recording level of the ATF PILOT signal controlling the ATF signal should be lower than the other signal by 2 dB when converted into the playback level. REC VCA changes the recording level.

The PLAREA signal from HD49211 controls this REC VCA circuit. The recording level is in the PILOT area when the PLAREA signal is "High", and in other areas when the signal is "Low".

The recording level is set according to four

external volumes. These are used for four cases: Ach in the PILOT or other area, and Bch in the PILOT or other area.

**Recording amplifier**

R-DAT recording is constant-current recording. The recording amplifier is switched on and off by the RECPB signal and SWH signal in the current amplifier which amplifies by about 40 dB (see interface block table) after voltage-current conversion of REC VCA output in external register R1. Since this amplifier output has an open-collector configuration, direct drive of the rotary transformer is possible.

The recording amplifier supplies the rotary transformer with an idling current about 12 mA from R2 for AC operation. Pin 25 has about 3.3 V and pin 24 and pin 43 have about 1 V. Dumping is done by Rd since the load is inductance. Rd uses series-connected resistors to reduce the influence of incidental capacitance.



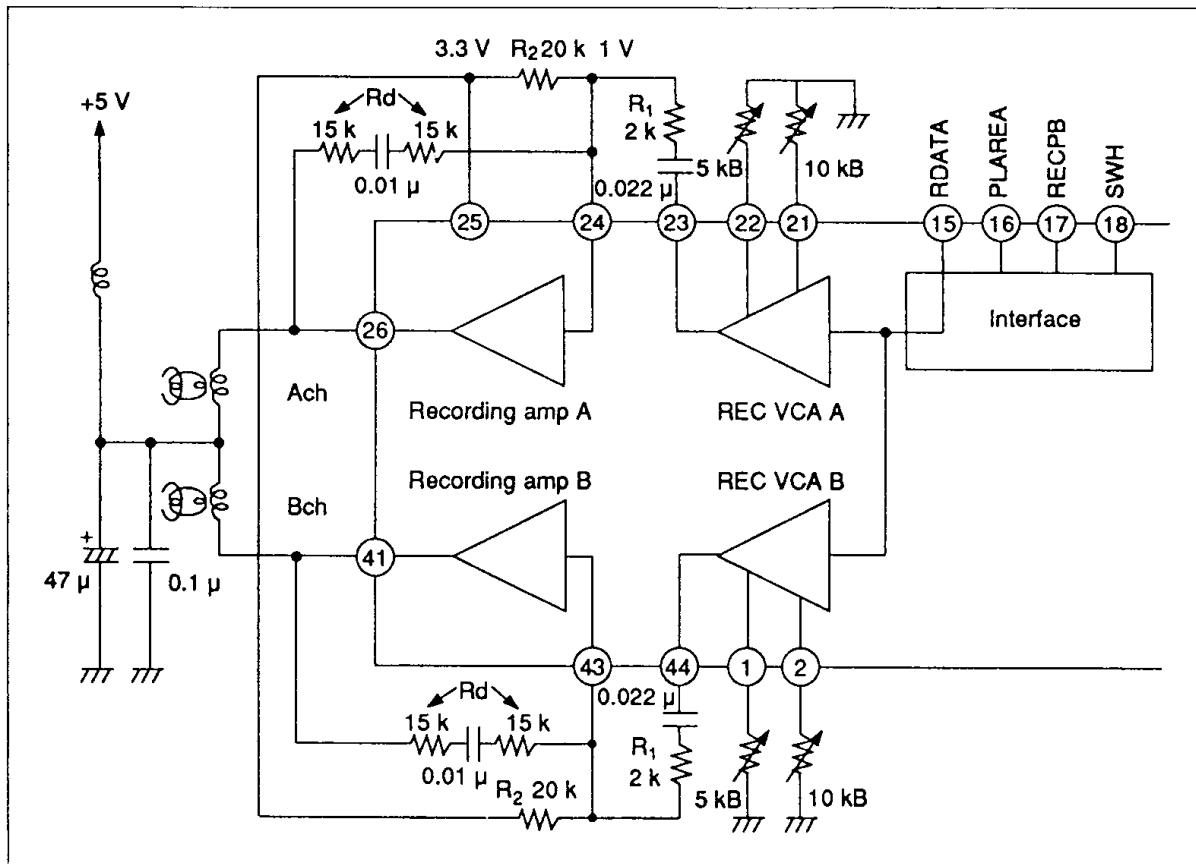


Figure 11 Recording Block

**Interface Block**

This interface block converts CMOS-level digital signals from HD49211 and HD49212 into ECL-

level signals which are used in this IC. Control signals for the preamplifiers and recording amplifiers are generated from RECPB and SWH signals.

Table 4 Interface Input Signal

RDATA	L	Recording data
	H	
PLAREA	L	Normal recording level
	H	ATF PILOT area recording level
RECPB	L	Playback mode (Recording amp is off)
	H	Recording mode (1st amp is off)
SWH	L	Selecting Ach
	H	Selecting Bch

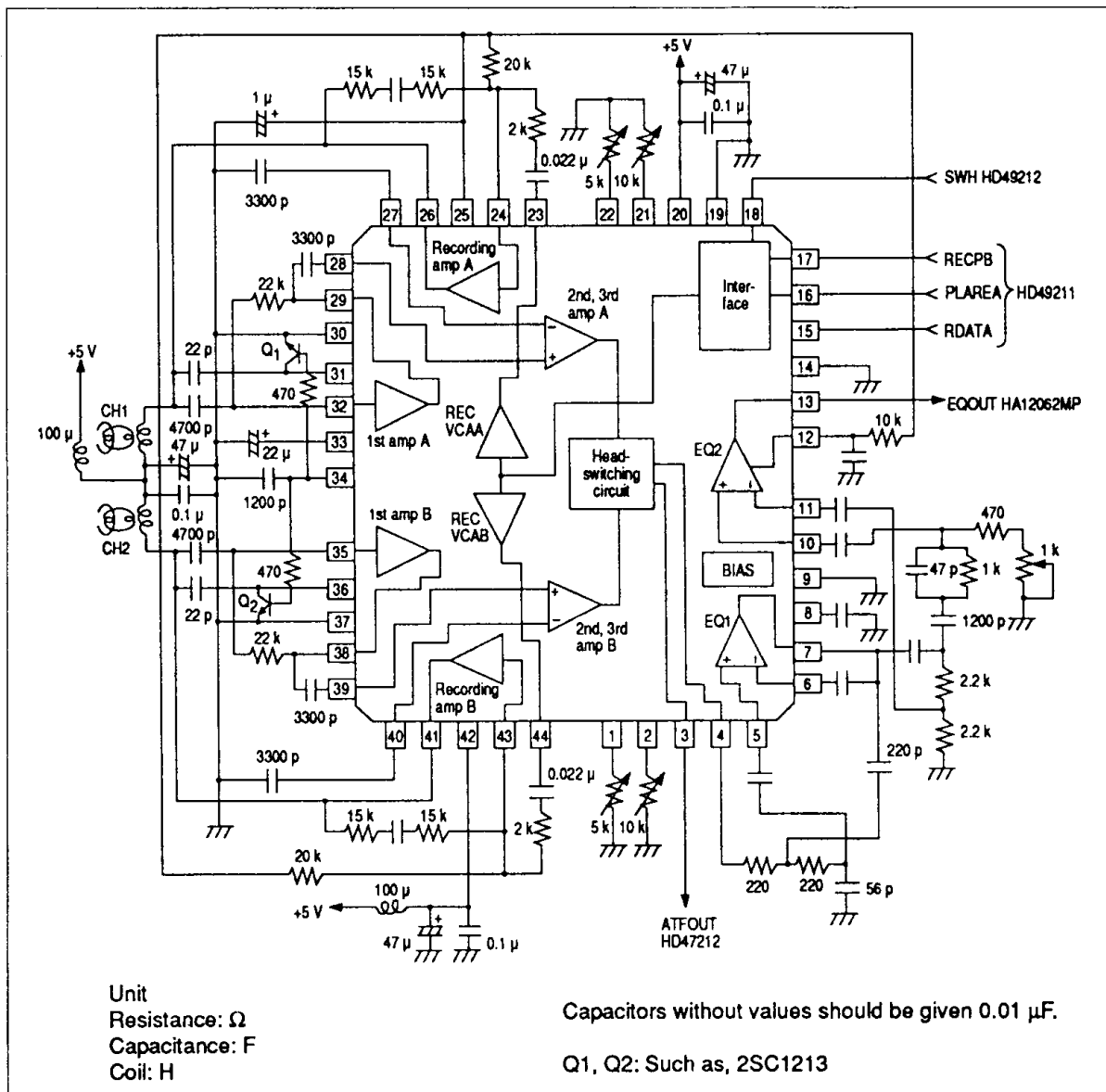


# HA12133MP

**Table 2 Preamp and Recording Amp Control**

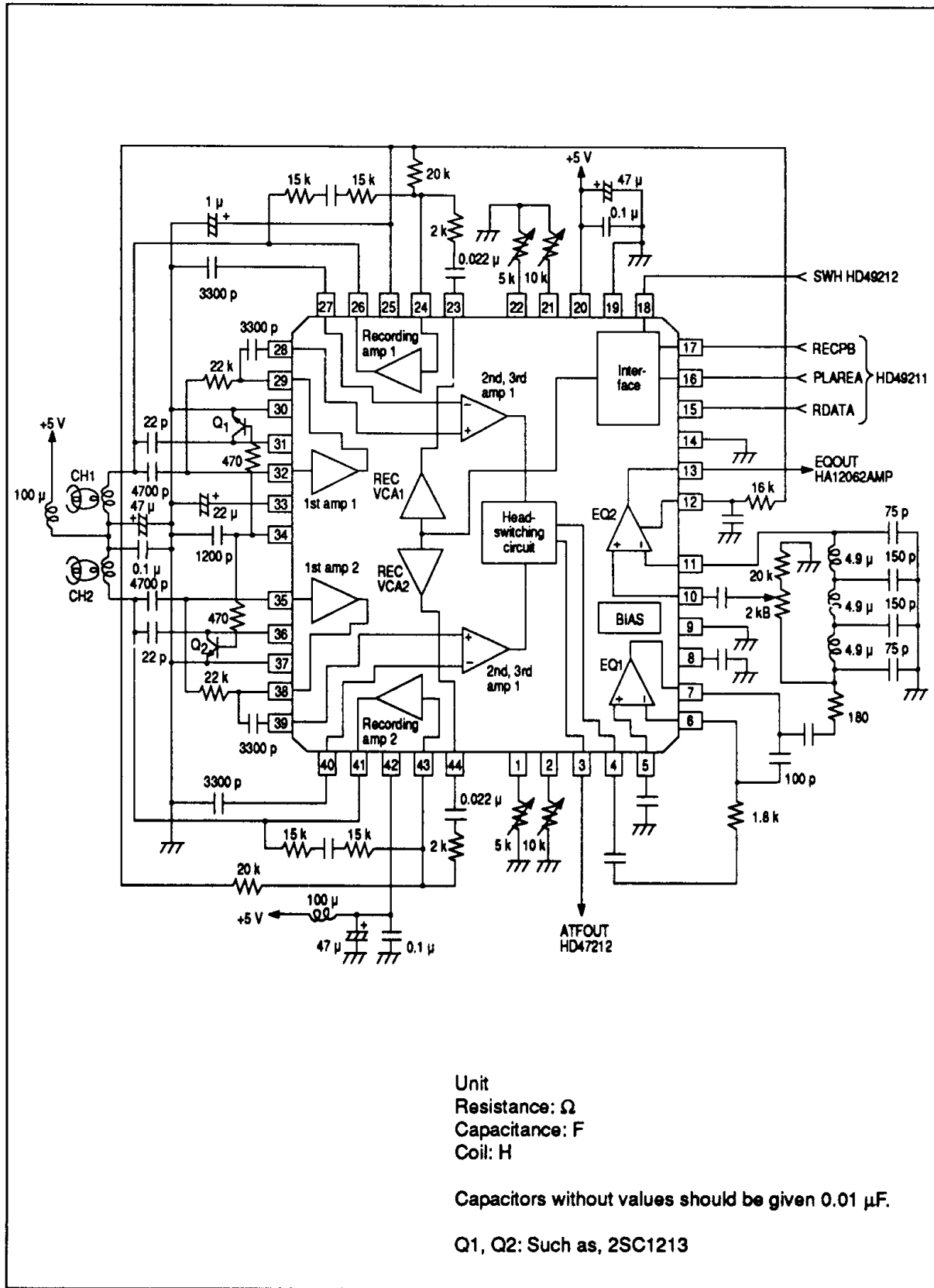
RECPB	SWH	Preamp	Recording amp	
			Ach	Bch
L	L	Selecting Ach	OFF	OFF
L	H	Selecting Bch	OFF	OFF
H	L	OFF	ON	OFF
H	H	OFF	OFF	ON

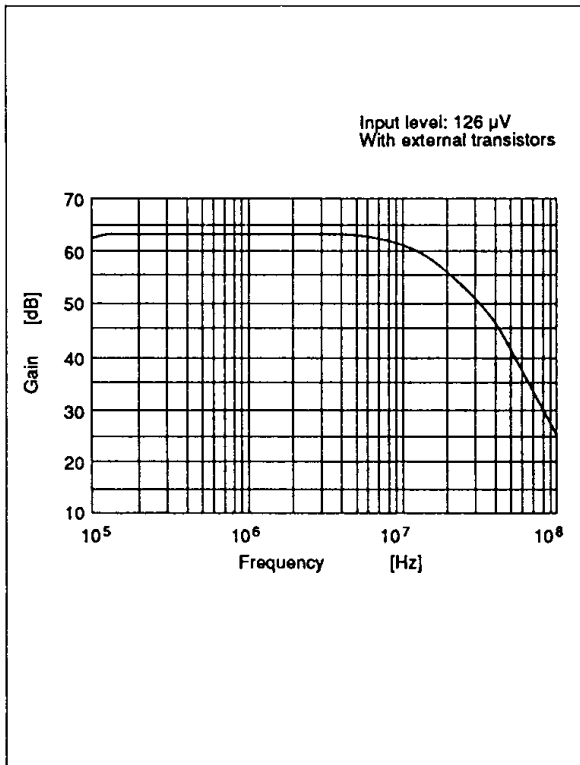
## Standard Application Circuit (1) CR-type Equalizer



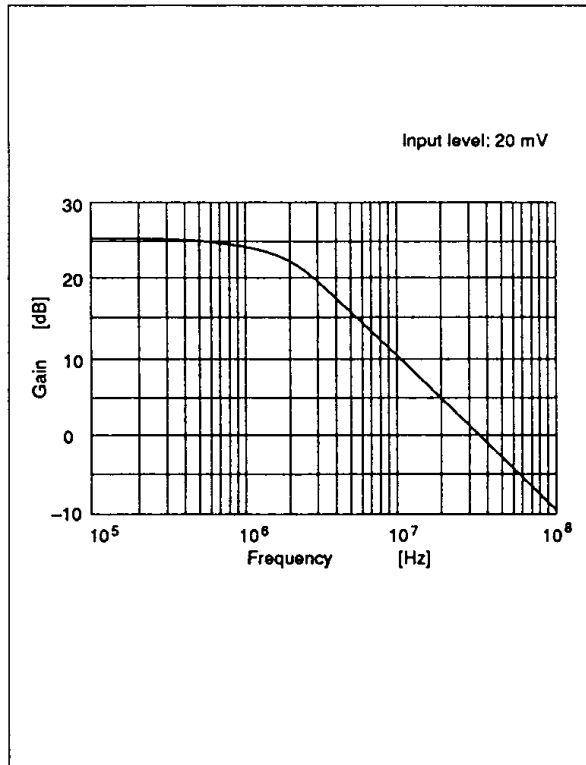


Standard Application Circuit (2) Reflector-type Transversal Equalizer

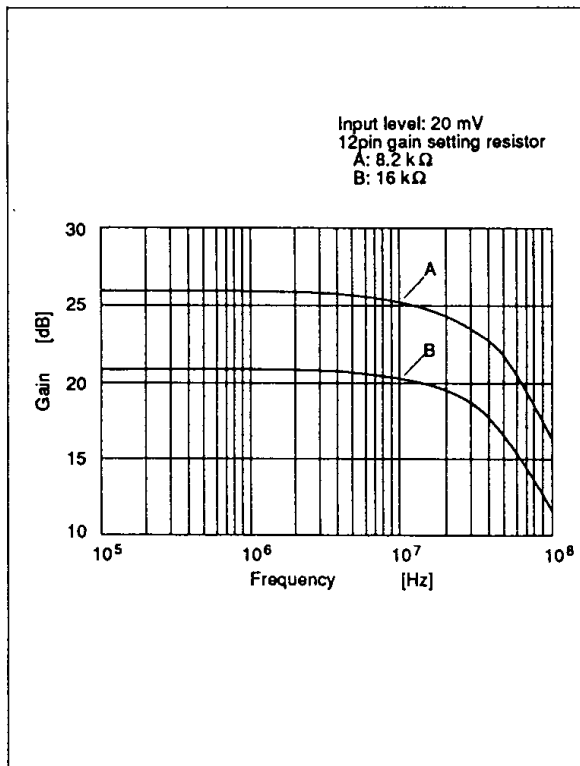




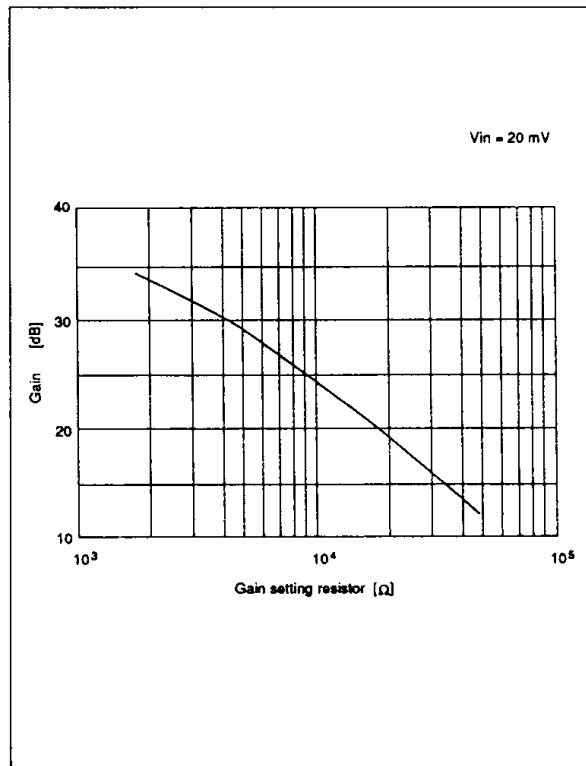
Preamp Frequency Characteristic



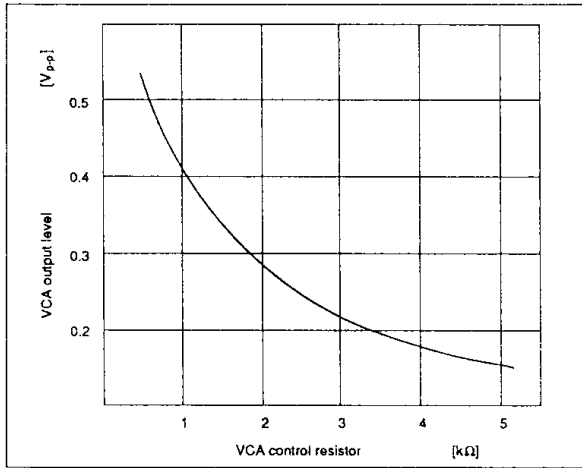
EQ1 Open Gain Frequency Characteristic



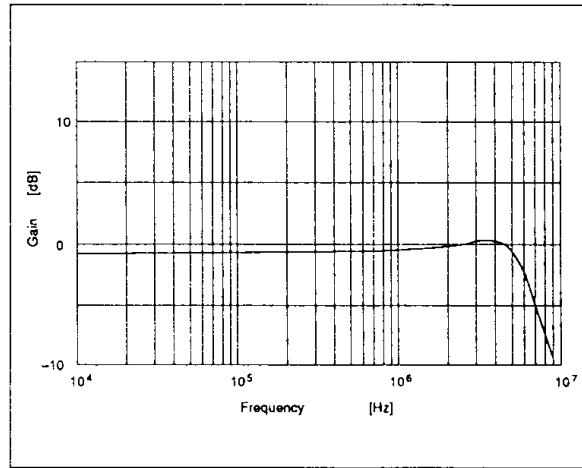
EQ2 Open Gain Frequency Characteristic



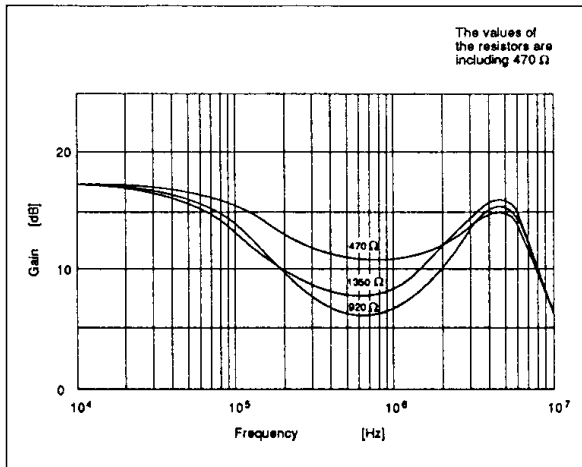
EQ2 Open Gain vs. Gain Setting Resistor



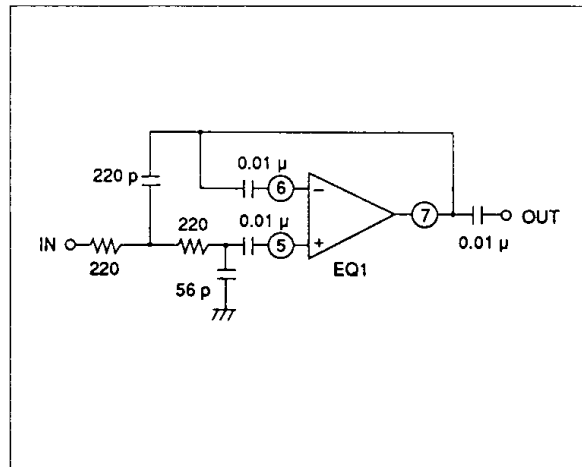
VCA Control Resistor vs. VCA Output level



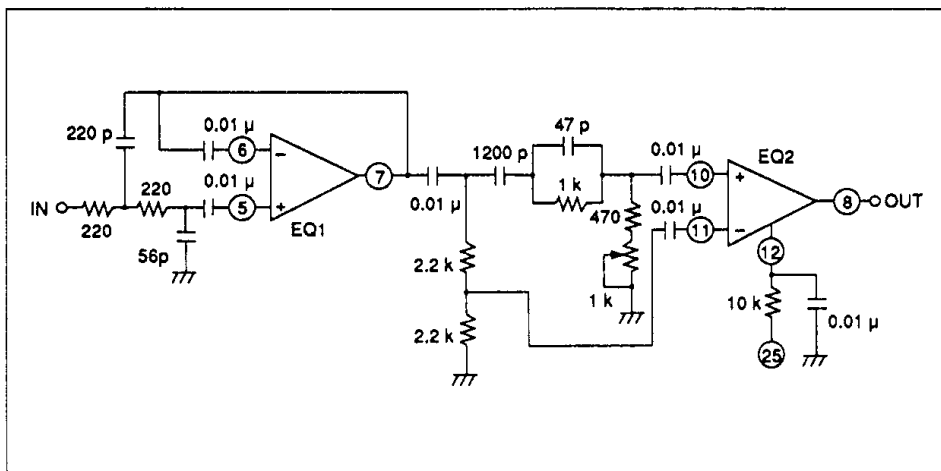
CR-type Equalizer LPF Frequency Characteristic (EQ1)



CR-type Equalizer Frequency Characteristic



CR-type Equalizer Frequency Characteristic Measuring Circuit



CR-type Equalizer Frequency Characteristic Measuring Circuit